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| Sheet | 1 | of | 3 | Application Number | 10/801,448 |
| | | | | Filing Date | March 12, 2004 |
| | | | | First Named Inventor | Phanindra K. Mannava |
| | | | | Art Unit | 2184 |
| | | | | Examiner Name | Not Yet Assigned |
| | | | | Attorney Docket Number | 42P17090 |

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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|-----------------------|----------------|--------------------|------------|
| Examiner Signature | /Charles Ehne/ | Date Considered | 10/10/2006 |
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NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.' | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T' |
|--------------------|-----------|---|----|
| CE | | US Application No.10/859,656 (Docket No.P18858); Title: Packet Exchange For Controlling System Power Modes; Inventor: Jeffery Wilcox; Filing Date: 6/2/2004. | |
| CE | | US Application No.10/956,630 (Docket No. P20125); Title: FAULT PROCESSING FOR DIRECT MEMORY ACCESS ADDRESS TRANSLATION; Inventor: Rajesh Madukkarumukumana; Filing Date: 9/30/2004 | |
| CE | | US Application No. 10/956,206 (Docket No. P20126); Title: CACHING SUPPORT FOR DIRECT MEMORY ACCESS ADDRESS TRANSLATION; Inventor: Ioannis Schoinas; Filing Date: 9/30/2004. | |
| CE | | US Application No. 10/956,198 (Docket No. P20127); Title: ADDRESS TRANSLATION FOR INPUT/OUTPUT DEVICES USING HIERARCHICAL TRANSLATION TABLES; Inventor: Ioannis Schoinas; Filing Date: 9/30/2004. | |
| CE | | US Application No. 10/957,306 (Docket No. P20128); Title: PERFORMANCE ENHANCEMENT OF ADDRESS TRANSLATION USING TRANSLATION TABLES COVERING LARGE ADDRESS SPACES; Inventor: Ioannis Schoinas; Filing Date: 9/30/2004. | |
| CE | | US Application No.11/011,300 (Docket No.P20265); Title: METHOD, SYSTEM, AND APPARATUS FOR DYNAMIC RECONFIGURATION OF RESOURCES; Inventor: Mani Ayyar; Filing Date: 12/13/2004. | |
| CE | | US Application No.11/011801 (Docket No.P20266); Title: METHOD, SYSTEM, AND APPARATUS FOR SYSTEM LEVEL INITIALIZATION; Inventor: Mani Ayyar; Filing Date: 12/13/2004. | |

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|--------------------|-----------|---|----------------|
| CE | | US Application No.11/026,314 (Docket No.P20926); Title: Direct Memory Access (DMA) Address Translation Between Peer Input/Output (I/O) Devices; Inventor: Rajesh Madukkarumukumana; Filing Date: 12/29/2004. | |
| CE | | US Application No.11/321,213 (Docket No.P21970); Title: FIRM PARTITIONING IN A SYSTEM WITH A POINT-TO-POINT INTERCONNECT; Inventor: Ioannis Schoinas; Filing Date: 12/28/2005. | |
| CE | | US Application No.11/284,520 (Docket No.P22379); Title: In Band Configuration Agent For Link Based Computing System; Inventor: Eric Delano; Filing Date: 11/21/2005. | |
| CE | | US Application No.11/320,923 (Docket No.P22868); Title: CONDITIONAL AND VECTORED SYSTEM MANAGEMENT INTERRUPTS; Inventor: Mani Ayyar; Filing Date: 12/28/2005. | |
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